What is claimed is:

1. A semiconductor device comprising:

a transistor having a first impurity region and a second impurity region formed on a semiconductor substrate, and a gate electrode formed on the semiconductor substrate;

a first insulating film for covering the transistor;

a capacitor formed on the first insulating film, the capacitor having a dielectric film formed of either ferroelectric material or high-dielectric material, and an upper electrode and a lower electrode positioned to put the dielectric film therebetween; and

a silicon oxide film formed over the capacitor and having its planarized surface, at least the planarized surface of the silicon oxide film including nitrogen.

2. A semiconductor device according to claim 1, wherein cavities are formed in an inside of the silicon oxide film.

3. A semiconductor device according to claim 1, further comprising,

a second insulating film formed between the capacitor and the silicon oxide film; and

a wiring formed on the second insulating film.

4. A semiconductor device according to claim 2, further comprising:

a third insulating film formed on the silicon oxide film.

5. A semiconductor device comprising:

a transistor having a first impurity region and a second impurity region formed on a semiconductor substrate, and a gate electrode formed on the semiconductor substrate;

a first insulating film for covering the transistor;

a capacitor formed on the first insulating film, the capacitor having a dielectric film formed of either ferroelectric material or high-dielectric material, and an upper electrode and a lower electrode positioned to put the dielectric film therebetween;

a second insulating film formed on the capacitor;

a local interconnection formed on the second insulating film, for electrically connecting the upper electrode of the capacitor to the first impurity region;

a third insulating film formed on the local interconnection and the second insulating film;

a first wiring formed on the third insulating film and electrically connected to the second impurity region via a hole which is formed on the first insulating film, the second insulating film, and the third insulating film;

a fourth insulating film formed on the first

wiring and having its upper planarized surface; and

a second wiring formed on the fourth insulating film.

6. A semiconductor device according to claim 5, wherein cavities, a part of which are exposed from the upper surface of the fourth insulating film, are formed in an inside of the fourth insulating film.

7. A semiconductor device according to claim 6, wherein the cavities are located in regions between a plurality of capacitors.

8. A semiconductor device according to claim 6, further comprising:

a fifth insulating film formed on the fourth insulating film to cover the cavities which are exposed from the upper surface of the fourth insulating film.

9. A semiconductor device according to claim 5, wherein the second wiring is connected to the first wiring via the hole formed in the fourth insulating film.

10. A semiconductor device according to claim 5, wherein the third insulating film and the fourth insulating film are formed of a silicon oxide film.

11. A semiconductor device according to claim 5, wherein an upper surface of the first insulating film is a planarized surface.

12. A semiconductor device comprising:

a transistor having a first impurity region and a

second impurity region formed on a semiconductor substrate, and a gate electrode formed on the semiconductor substrate;

a first insulating film for covering the transistor;

a capacitor formed on the first insulating film, the capacitor having a dielectric film formed of either ferroelectric material or high-dielectric material, and an upper electrode and a lower electrode positioned to put the dielectric film therebetween;

a second insulating film covering the capacitor; and

wherein a surface of the second insulating film is planarized and plasma annealed.

13. A method of manufacturing a semiconductor device comprising the steps of:

forming a transistor on a semiconductor substrate;

forming a first insulating film on the semiconductor substrate to cover the transistor;

forming a capacitor, which includes a dielectric film formed of either a ferroelectric material or a high- dielectric material and an upper electrode and a lower electrode formed to put the dielectric film therebetween, on the first insulating film;

forming a second insulating film over the capacitor;

planarizing an upper surface by polishing the second insulating film; and

applying a dehydration process to the second insulating film by plasma annealing.

14. A method according to claim 13, wherein the plasma annealing is performed by plasmanizing a single gas of one of N_2O, N_2, NO, and O_2, or a mixed gas including one of N_2O, N_2, NO and O_2.

15. A method of manufacturing a semiconductor device according to claim 13, wherein the second insulating film is formed by a plasma enhanced CVD method using a TEOS gas.

16. A method of manufacturing a semiconductor device according to claim 13, wherein cavity is formed in the second insulating film.

17. A method of manufacturing a semiconductor device according to claim 16, wherein upper portions of the cavity is exposed by polishing the second insulating film.

18. A method of manufacturing a semiconductor device according to claim 13, further comprising the step of:

forming a third insulating film on the second insulating film after the dehydration process.

19. A method of manufacturing a semiconductor device according to claim 13, further comprising the step of:

forming a fourth insulating film between the capacitor and the second insulating film to cover the capacitor; and

forming a wiring between the second insulating film and the fourth insulating film.